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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FRANCISCO JAVIER GUERRERO MERCADO

Appeal 2008-3657
Application 10/619,169[1]
Technology Center 2800

Decided:[2] January 30, 2009

Before KENNETH W. HAIRSTON, ROBERT E. NAPPI,
and MARC S. HOFF, *Administrative Patent Judges*.

HOFF, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] Application filed July 14, 2003. The real party in interest is National Semiconductor Corporation.

[2] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

STATEMENT OF CASE

Appellant appeals under 35 U.S.C. § 134 from a Final Rejection of claims 1-3, 7-11, and 15-20.[3] We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Appellant's invention relates to an integrated circuit comparator consuming limited power while having reduced propagation delay (Spec. 2-3). A pulsed rather than continuous bias current is applied to a current source within the comparator's input gain stage (Spec. 4). The pulse width of the bias current is small relative to the system clock, but has a large current magnitude (Spec. 4).

Claim 1 is exemplary:

1. An integrated circuit comparator comprising:

an input receiving an input signal representative of a difference between quantities to be compared; and

an input gain stage receiving the input signal and biased with a pulsed bias current, the input gain stage producing a gain based upon the input signal.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Lim	US 5,841,306	Nov. 24, 1998
Heinrich	US 6,323,695	Nov. 27, 2001

Adel S. Sedra, *Microelectronic Circuits*, 3rd ed., pp. 220-222, 337-347, (1989).

[3] Claims 4-6 and 12-14 are objected to as being dependent upon a rejected base claim, but indicated as allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims.

Claims 7, 8, and 15-20 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement.

Claims 1-3, 10, and 11 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Lim.

Claims 1-3, 8-11, 16, and 17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Heinrich.

Rather than repeat the arguments of Appellant or the Examiner, we make reference to the Appeal Brief (filed June 11, 2007), the Reply Brief (filed September 25, 2007), and the Examiner's Answer (mailed July 23, 2007) for their respective details.

ISSUES

There are three principal issues in the appeal before us.

1. Did the Examiner err in concluding that Appellant did not have possession of the subject matter recited in claims 7, 8, and 15-20?

2. Did the Examiner err in finding that Lim teaches an input gain stage receiving the input signal and biased with a pulsed bias current?

3. Did the Examiner err in finding that Heinrich teaches an input gain stage receiving the input signal and biased with a pulsed bias current?

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

The Invention

1. According to Appellant, the invention concerns an integrated circuit comparator consuming limited power while having reduced

propagation delay (Spec. 2-3). A pulsed rather than continuous bias current is applied to a current source within the comparator's input gain stage (Spec. 4).

2. Appellant's Summary of the Invention states that "[T]he pulse with (*sic*, width) of the bias current is small relative to the system clock, but has a large current magnitude allowing the comparator to quickly respond to applied voltages, but without unacceptable increase in current and power consumption" (para. 0006).

3. Appellant's Specification further states that "[t]he comparator's average power consumption in pulsed bias current mode depends on the ration (*sic*, ratio) between pulse_w and t_sample. For a small pulse_w/t_sample ratio, the comparator's average power consumption will be similar to the value of the low power slow comparator configuration's" (para. 0030).

4. The Specification provides an exemplary width of the current pulses as 390 ns (para. 0026, 0027). The system clock employed has a period of 10 µs, giving a bias current pulse to clock period ratio of 390 ns/10 µs, or 3.9% (para. 0027).

Lim

5. Lim teaches a pulse generator that generates a pulse signal having a desired width regardless of the width of a trigger input (col. 2, ll. 7-9).

6. Lim teaches a power saving mode (corresponding to interval t3 in Fig. 5) in which bias current is not provided (Fig. 5; col. 4, ll. 32-57).

Heinrich

7. Heinrich teaches a comparator having a controllable bias current source for supplying a bias current having a low quiescent current strength or a higher active current strength as a function of whether the input signal is constant or variable (col. 1, ll. 36-40).

Sedra

8. Sedra teaches that transconductance is directly proportional to the collector current of a bipolar transistor (Sedra, 222).

PRINCIPLES OF LAW

Under the written description requirement of 35 U.S.C. § 112, the disclosure of the application relied upon must reasonably convey to one of ordinary skill in the art that, as of the filing date of the application, the inventor had possession of the later-claimed subject matter. *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563 (Fed. Cir. 1991). "One shows that one is 'in possession' of *the invention* by describing *the invention,* with all its claimed limitations, not that which makes it obvious." *Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997) (emphasis in original).

"A rejection for anticipation under section 102 requires that each and every limitation of the claimed invention be disclosed in a single prior art reference." *See In re Buszard*, 504 F.3d 1364, 1366 (Fed. Cir. 2007) (quoting *In re Paulsen*, 30 F.3d 1475, 1478-79 (Fed. Cir. 1994)). "Anticipation of a patent claim requires a finding that the claim at issue 'reads on' a prior art reference." *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed. Cir. 1999) (quoting *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 781 (Fed. Cir. 1985)).

Analysis of whether a claim is patentable over the prior art under 35 U.S.C. § 102 begins with a determination of the scope of the claim. We determine the scope of the claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004). The properly interpreted claim must then be compared with the prior art.

The claim terms should be given their broadest reasonable meaning in their ordinary usage as such claim terms would be understood by one skilled in the art by way of definitions and the written description. *In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997).

> "The claims, of course, do not stand alone. Rather, they are part of a 'fully integrated written instrument' . . . consisting principally of a specification that concludes with the claims. For that reason, claims 'must be read in view of the specification, of which they are a part.' . . . [T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'"

Phillips v. AWH Corp., 415 F.3d 1303, 1315 (Fed. Cir. 2005).

Our reviewing court states that "claims must be interpreted as broadly as their terms reasonably allow." *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989). Our reviewing court further states that "the words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.*, 415 F.3d at 1312 (en banc)(internal citations omitted). The "ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at

1313. The description in the specification can limit the apparent breadth of a claim in two instances: (1) where the specification reveals a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess; and (2), where the specification reveals an intentional disclaimer, or disavowal, of claim scope by the inventor. *Id.* at 1316.

ANALYSIS

Rejection under 35 U.S.C. § 112, first paragraph

The Examiner alleges that claims 7, 8, and 15-20 lack enablement because the specification fails to describe how "'the pulsed bias current comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock,'" as claim 7 requires. In the Examiner's view, the absence of a displayed clock signal from pulse generator 301 and comparator 100 (in Figures 3 and 1, respectively) indicates that Appellant did not have possession of the invention as of the filing date (Ans. 3).

We are persuaded by Appellant's position, however, that it was known in the art as of the filing date of the application that system clocks are well known in the art to control various components or logical units within an integrated circuit (App. Br. 8), and that such clocks are generally not depicted in high level drawings (App. Br. 9). Further, we agree with Appellant that, at the time the application was filed, the use of a clock edge (whether rising or falling) to trigger an event or action was also well known (App. Br. 9). We therefore find that Appellant need not have illustrated such a known system clock in the Figures, nor described how such known edge-

triggering is accomplished, in order to show that he had possession of the invention as of the filing date of the application. We find error in the Examiner's rejection of claims 7, 8, and 15-20 under 35 U.S.C. § 112, first paragraph.

With respect to claims 8 and 17, the Examiner argues that the Specification does not describe how *selection* of a first comparator mode having a first level of bias current, as opposed to a second mode having a second level of bias current, is achieved (Ans. 8). Appellant points out in response, however, that the claims do not affirmatively require such selection; the claims in fact require that the claimed comparator "selectively operates in a first mode ... or in a second mode" (Reply Br. 6-7). We agree with Appellant that the phrase "selectively operates" in claims 8 and 17 requires only that "the comparator be capable of operating in different modes" (Reply Br. 6). Whether the specification describes the selection process is, therefore, not relevant to the question of whether Appellant had possession of the claimed invention as of the filing of the application. Because the Examiner has not shown that any element of claims 8 or 17 lacks enablement, we find error in the Examiner's rejection of claims 8 and 17 under 35 U.S.C. § 112, first paragraph.

With respect to claim 19, the Examiner asserts that the Specification does not disclose "how to implement a circuit in which the parameter gm is generated and a current source is controlled by the parameter gm in producing the pulsed or continuous bias current" (Ans. 9). The Examiner's rejection is erroneous, however, because the Sedra reference, cited by the Examiner to teach that transconductance parameter gm may be produced across the collector and emitter of a bipolar transistor, teaches that it is

known that transconductance is directly proportional to the collector current of a bipolar transistor (FF 8). Because Sedra teaches that it is well known to vary transconductance by varying collector current, we conclude that it was error for the Examiner to reject claim 19 under 35 U.S.C. § 112, first paragraph, based on the Specification's lack of disclosure of a known principle.

We thus reverse the Examiner's rejection of claims 7, 8, and 15-20 under 35 U.S.C. § 112, first paragraph.

§ 102 rejection over Lim[4]

Independent claims 1 and 9 both require an input gain stage "biased with a pulsed bias current." The Examiner argues that Lim anticipates claims 1-3, 10, and 11, because in the Examiner's interpretation, independent claims 1 and 9 "do not call for pulsed bias current – that is, a current that is pulsed in accordance with a system clock" (Ans. 9).

We begin by reading the claims in light of the specification, as the *Phillips* court commands. Appellant's Specification makes clear that a (very) short duration pulse of the bias current is contemplated. Appellant wishes to quickly respond to applied voltages without consuming large amounts of power. Appellant's Summary of the Invention states that "[T]he pulse with (*sic*, width) of the bias current is small relative to the system clock but has a large current magnitude allowing the comparator to quickly respond to applied voltages, but without unacceptable increase in current and power consumption" (FF 2). Appellant's Specification further states that

[4] We note that the Examiner's rejection over Lim includes claims 10 and 11, but not independent claim 9 from which claims 10 and 11 depend. We will treat the Examiner's rejection over Lim as though claim 9 were included.

"[t]he comparator's average power consumption in pulsed bias current mode depends on the ration (*sic*, ratio) between pulse_w and t_sample. For a small ratio, the comparator's average power consumption will be similar to the value of the low power slow comparator configuration's" (FF 3).

Figures 2B and 2C illustrate operation of comparator 100 in fast comparator configuration, but with a pulsed bias current. The Specification makes reference to the exemplary width of the current pulses as 390 ns (FF 4). The system clock employed has a period of 10 us, giving a bias current pulse to clock period ratio of 390 ns/10 us or 3.9% (FF 4).

As a result of the evidence cited *supra*, we find that Appellant's Specification "limits the apparent breadth of the claim" by revealing "a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess," *Phillips*, 415 F.3d at 1316. Specifically, we construe "pulsed bias current" as limited to a current pulsed *in accordance with a system clock*.

Applying this claim construction to the prior art applied by the Examiner, we do not agree with the Examiner that Lim teaches an input gain stage biased with a pulsed bias current. Rather than teaching a bias current pulsed in accordance with a system clock, Lim merely teaches a power saving mode (corresponding to interval t3 in Fig. 5) in which bias current is not provided (FF 6). Lim contains no teaching that a bias current having a pulse width which is small in comparison to the width of the system clock is provided. As noted *supra*, Appellant desires a small pulse width having a large magnitude in order to achieve fast comparator response without high comparator power consumption. A pulse width of the duration illustrated in

Lim Fig. 5C, which would have a very high ratio between pulse_w and t_sample, would thoroughly frustrate Appellant's objectives.

Because we find that Lim does not teach an input gain stage biased with a pulsed bias current, according to the claim construction explained *supra*, we find error in the Examiner's rejection of independent claims 1 and 9, as well as claims 2, 3, 10, and 11 dependent therefrom, under 35 U.S.C. § 102 as being anticipated by Lim.

§ 102 rejection over Heinrich

Each of independent claims 1, 9, and 17 recites a comparator input gain stage that is biased with a pulsed bias current. The Examiner argues that because the current Ic1 in Figure 3 of Heinrich has "a pulse shape waveform," Heinrich teaches all the limitations of independent claims 1, 9, and 17 (Ans. 10).

However, as explained with respect to the Examiner's rejection over Lim, *supra*, we construe "pulsed bias current," in light of the Specification, as limited to a current pulsed *in accordance with a system clock*. While Heinrich *is* directed to a comparator with a controllable bias current source, Heinrich does not teach a current pulsed in accordance with a system clock, or a current pulse having a short duration relative to the period of the system clock. Heinrich's teaching of a current with a "pulse shape waveform" is not sufficient to meet the claim construction we have explained.

Because Heinrich does not teach all the limitations of independent claims 1, 9, or 17, we find error in the Examiner's rejection of those claims, as well as claims 2, 3, 9-11, and 16 dependent therefrom, under 35 U.S.C. § 102 as being anticipated by Heinrich.

CONCLUSIONS OF LAW

The Examiner erred in finding that Appellant was not in possession of the invention as of the filing date of the application.

The Examiner erred in finding that Lim teaches an input gain stage receiving the input signal and biased with a pulsed bias current.

The Examiner erred in finding that Heinrich teaches an input gain stage receiving the input signal and biased with a pulsed bias current.

ORDER

The Examiner's rejection of claims 1-3, 7-11, and 15-20 is reversed.

REVERSED

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